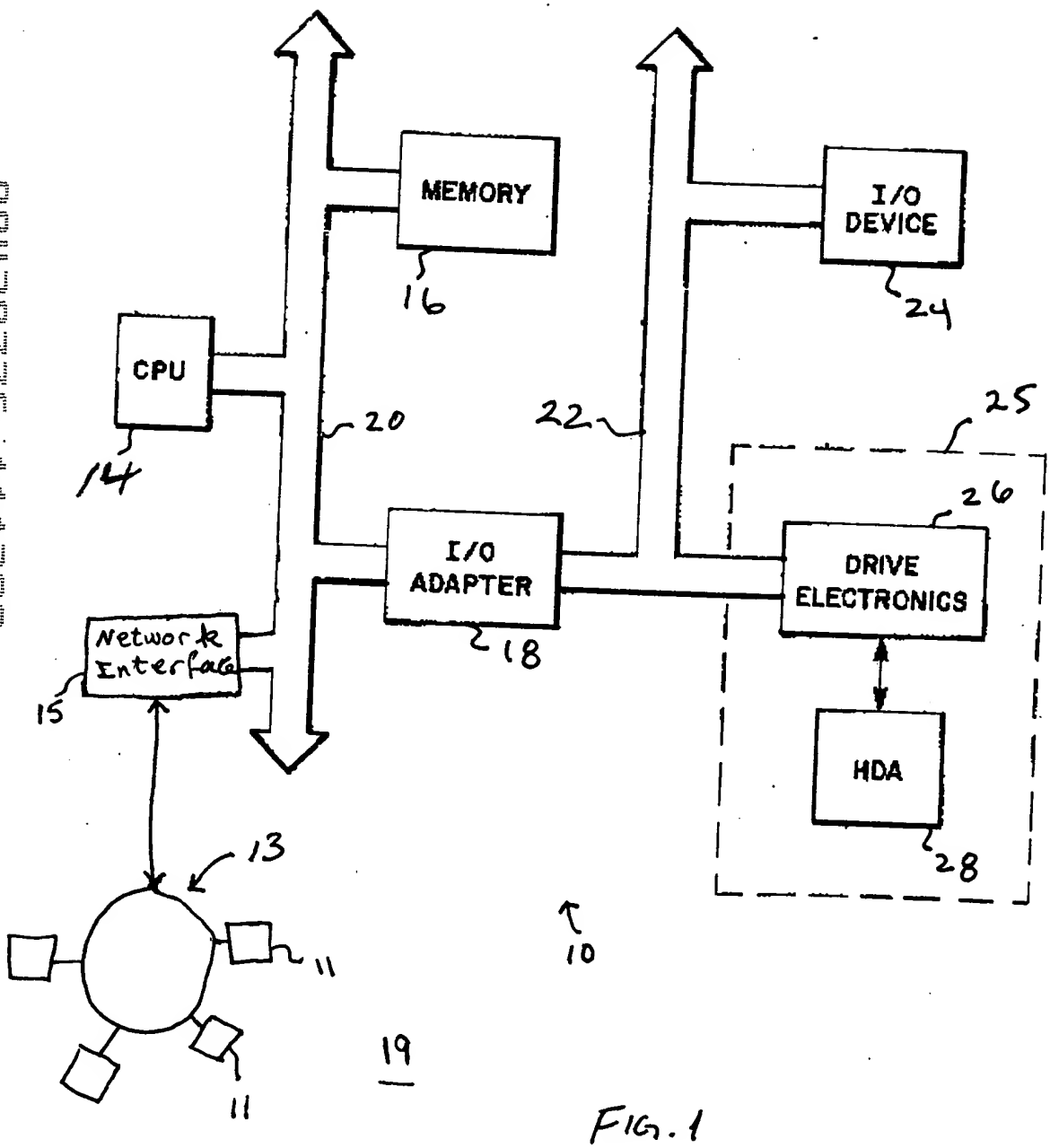

MEMORY
16
I/O DEVICE
24
CPU
14
20
22
25
26
I/O ADAPTER
18
DRIVE ELECTRONICS
Network Interface
15
HDA
28
13
11
11
19
10

FIG. 1

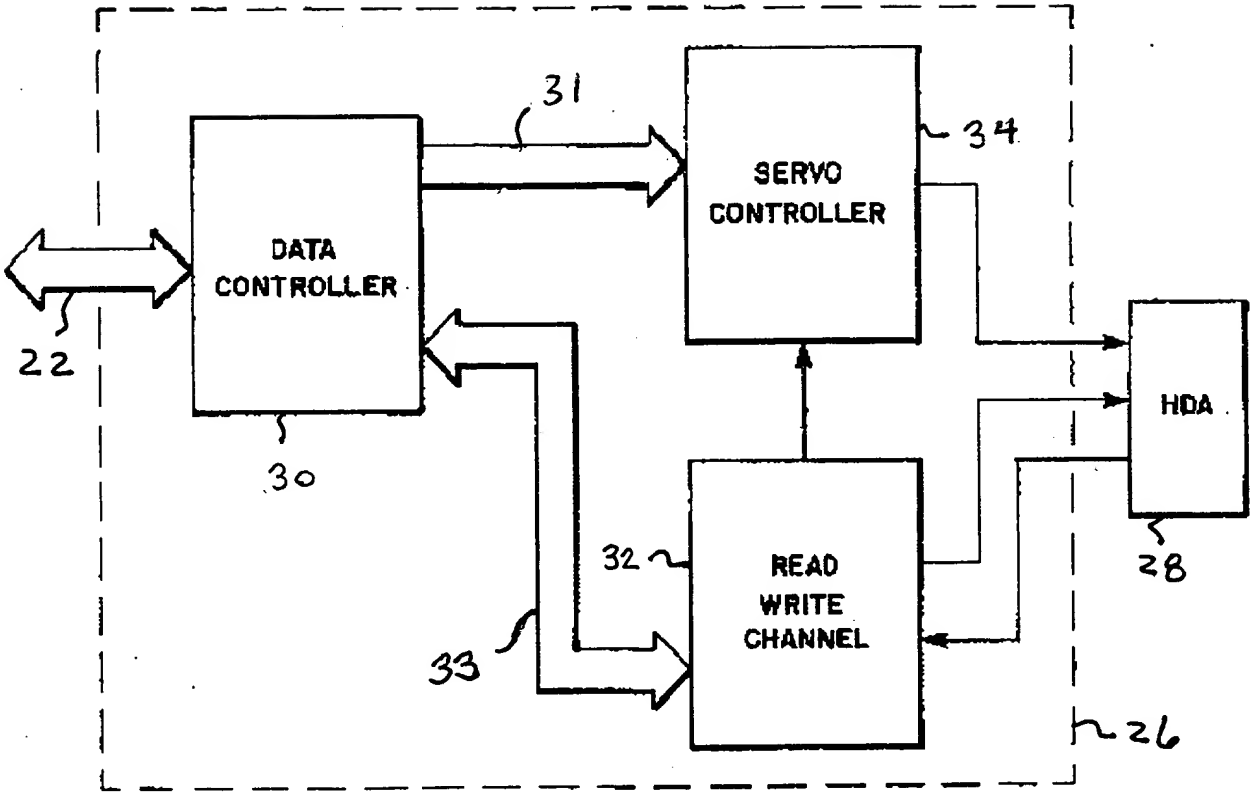


FIG. 2

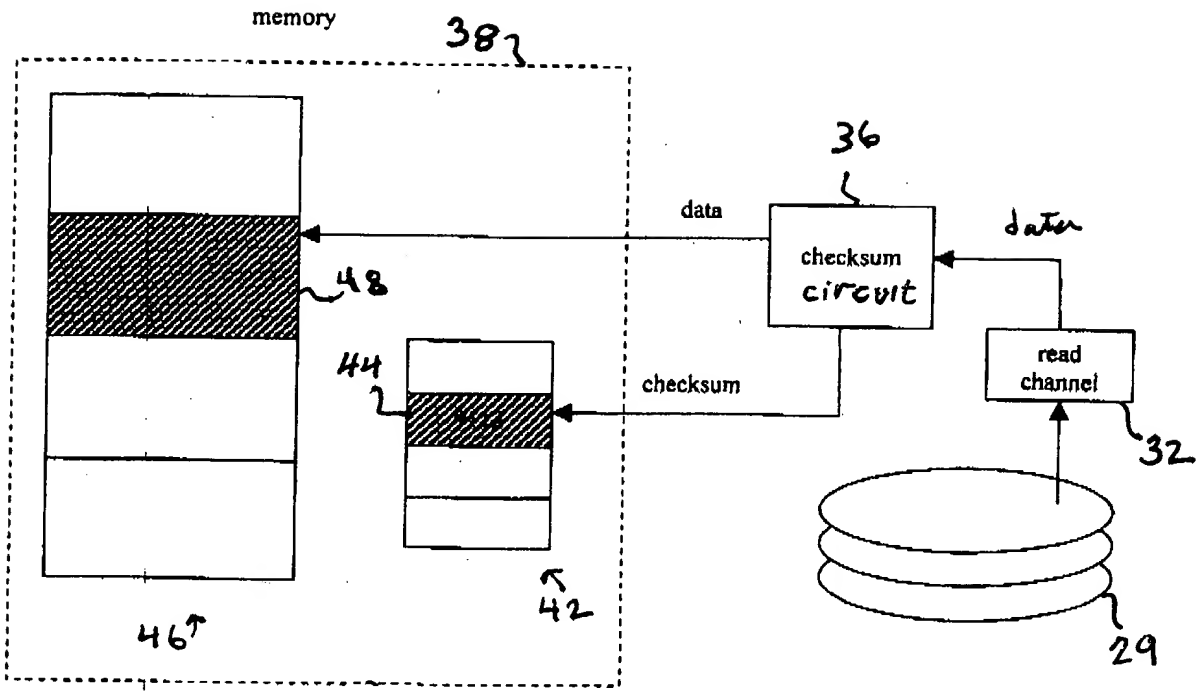

memory
38
36
data
checksum
circuit
data
48
44
checksum
read
channel
32
42
46
29
30

FIG. 3

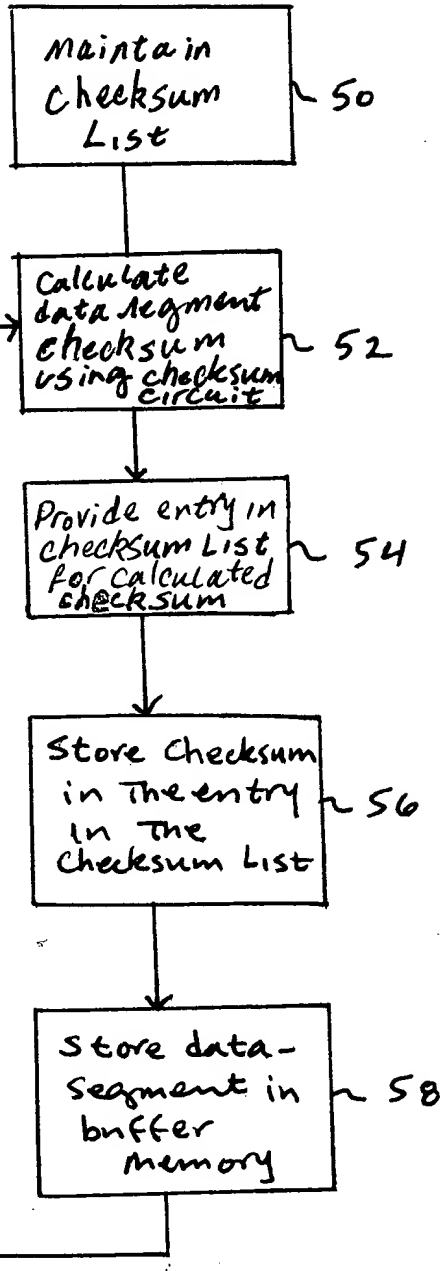

Maintain Checksum List
50
Calculate data segment checksum using checksum circuit
52
Provide entry in checksum List for calculated checksum
54
Store Checksum in The entry in The Checksum List
56
Store data-segment in buffer memory
58

FIG. 4

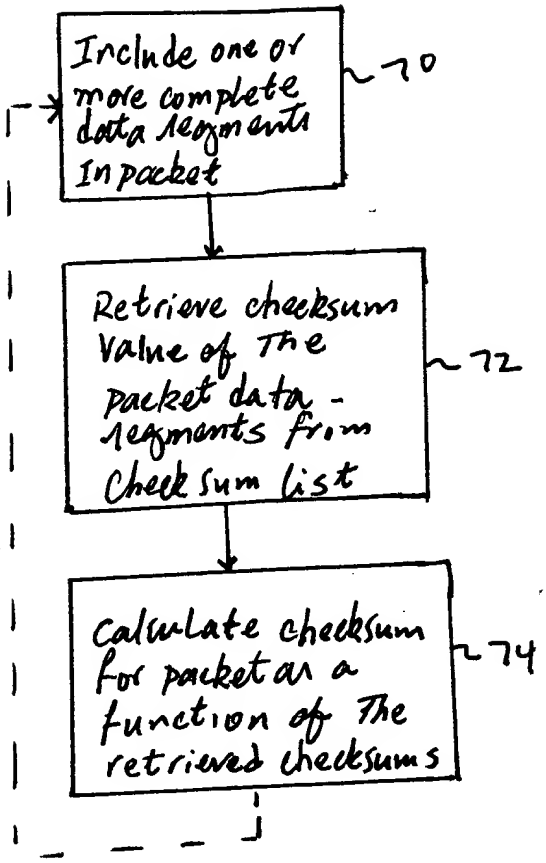

Include one or more complete data segments In packet
70
Retrieve checksum value of The packet data-segments from Check Sum list
72
Calculate checksum for packet as a function of The retrieved checksums
74

FIG. 6

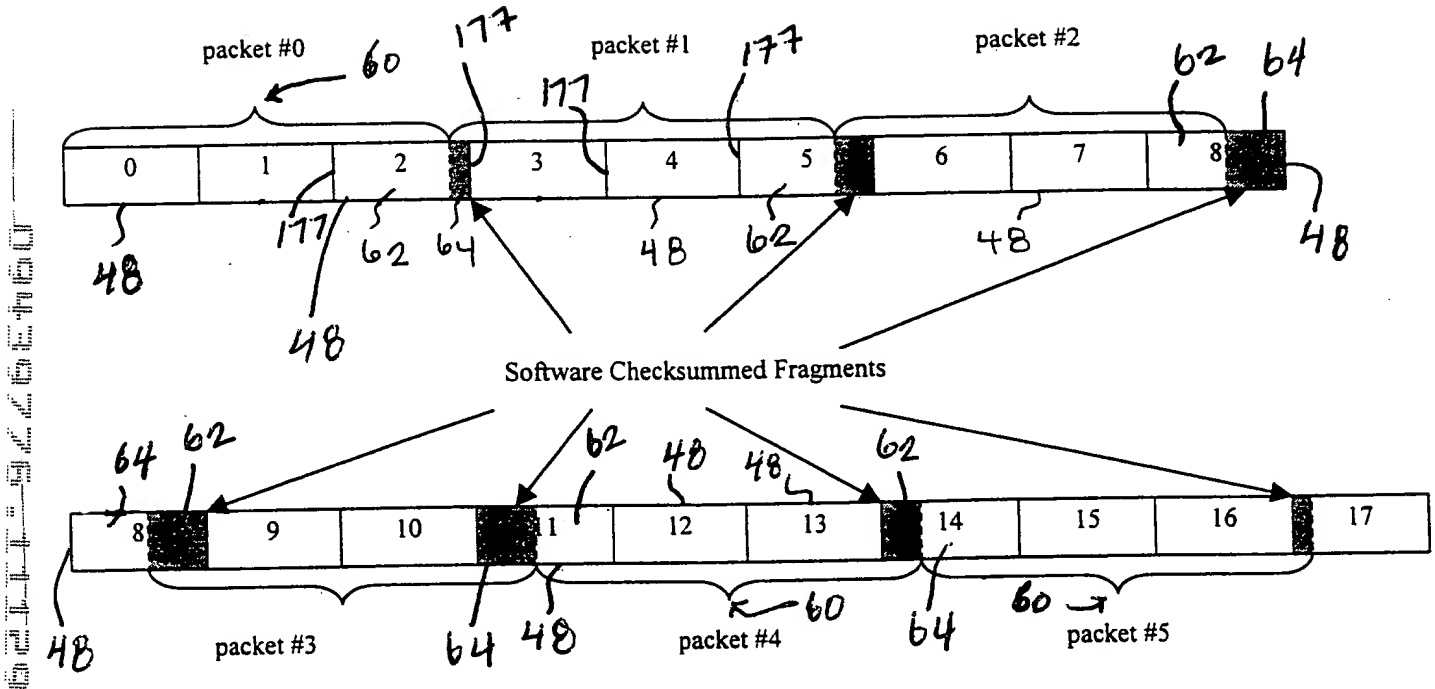


FIG. 5A

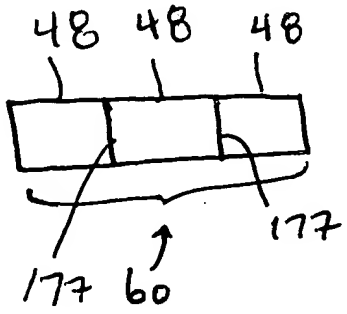


FIG. 5B

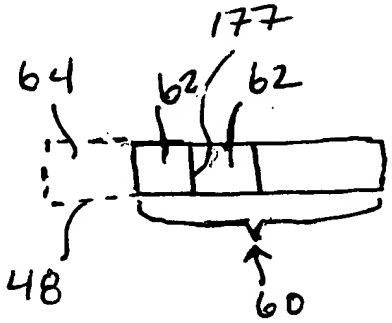


FIG. 5C

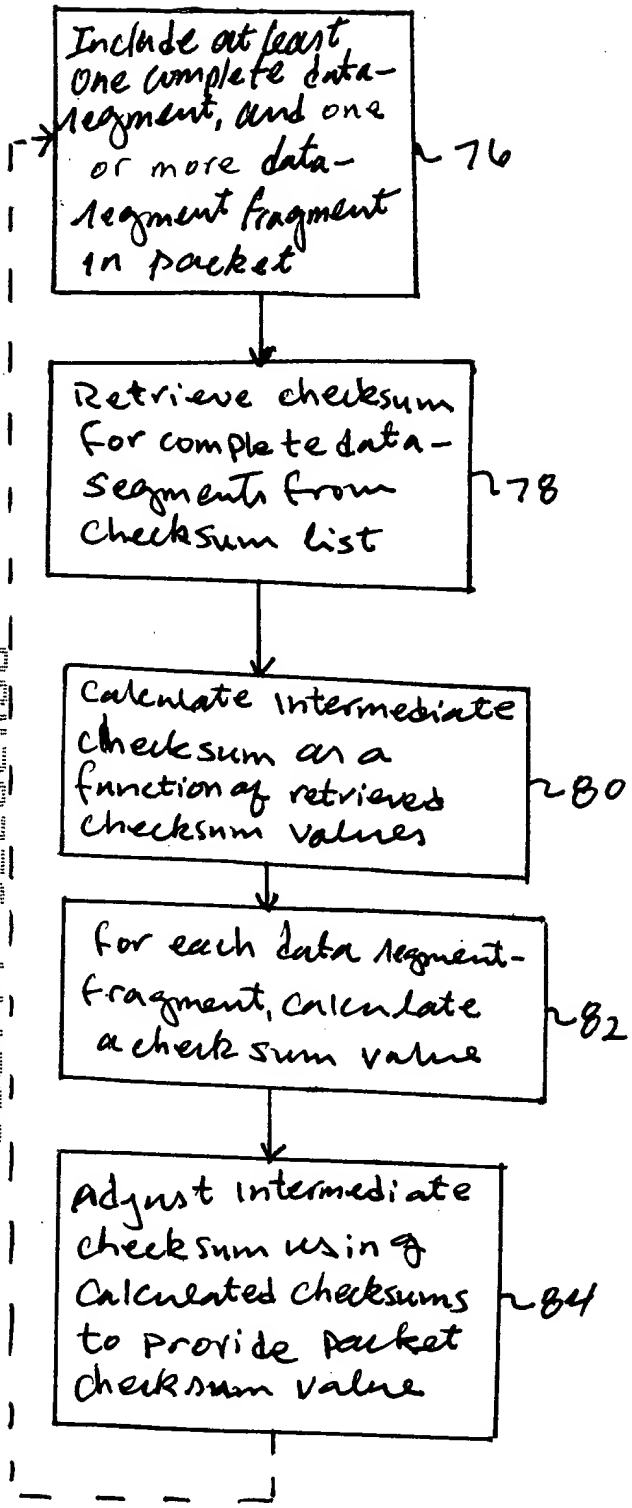

Include at least one complete data-segment, and one or more data-segment fragment in packet
76
Retrieve checksum for complete data-segments from checksum list
78
Calculate intermediate checksum as a function of retrieved checksum values
80
For each data segment-fragment, calculate a checksum value
82
Adjust intermediate checksum using calculated checksums to provide packet checksum value
84

FIG. 7A

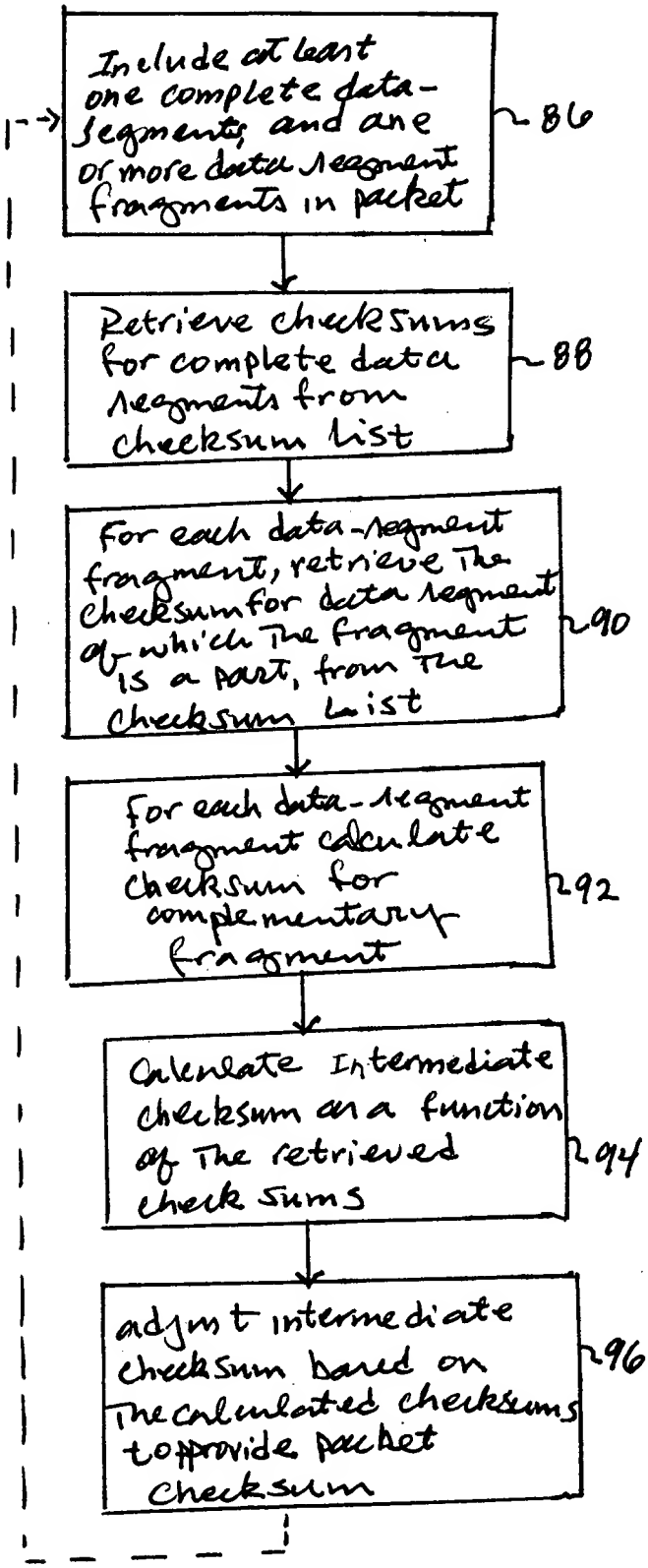

Include at least one complete data-segments, and one or more data segment fragments in packet
86
Retrieve checksums for complete data segments from checksum list
88
For each data-segment fragment, retrieve the checksum for data segment of which the fragment is a part, from the checksum list
90
For each data-segment fragment calculate checksum for complementary fragment
92
Calculate intermediate checksum as a function of the retrieved check sums
94
adjust intermediate checksum based on the calculated checksums to provide packet checksum
96

FIG. 7B

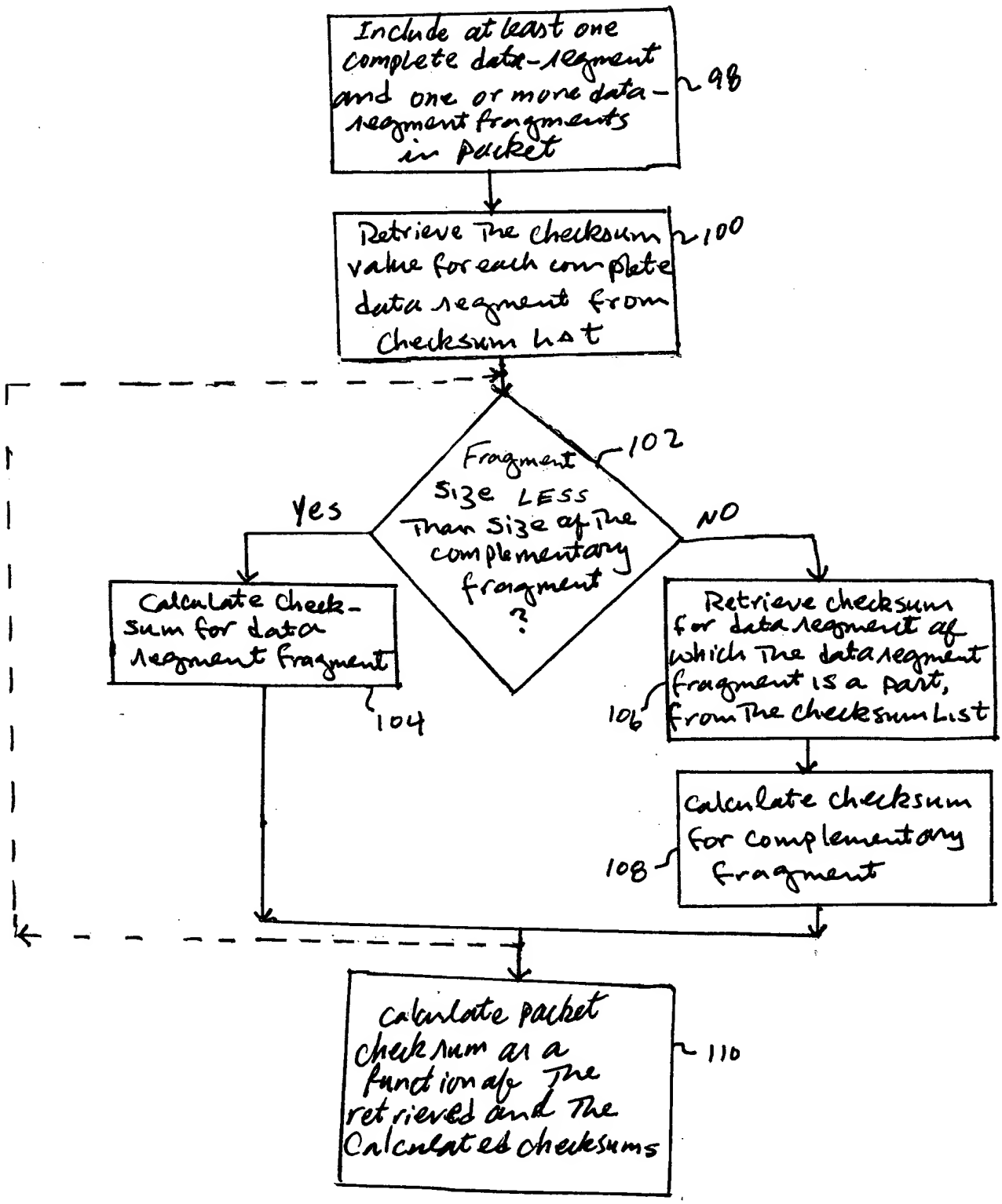

Include at least one complete data-segment and one or more data-segment fragments in packet
98
Retrieve the checksum value for each complete data segment from Checksum List
100
Fragment Size LESS Than Size of the complementary fragment ?
102
Yes
NO
Calculate Checksum for data segment fragment
104
Retrieve checksum for data segment of which the data segment fragment is a part, from the Checksum List
106
Calculate checksum for complementary fragment
108
Calculate packet checksum as a function of the retrieved and the Calculated checksums
110

FIG. 7c

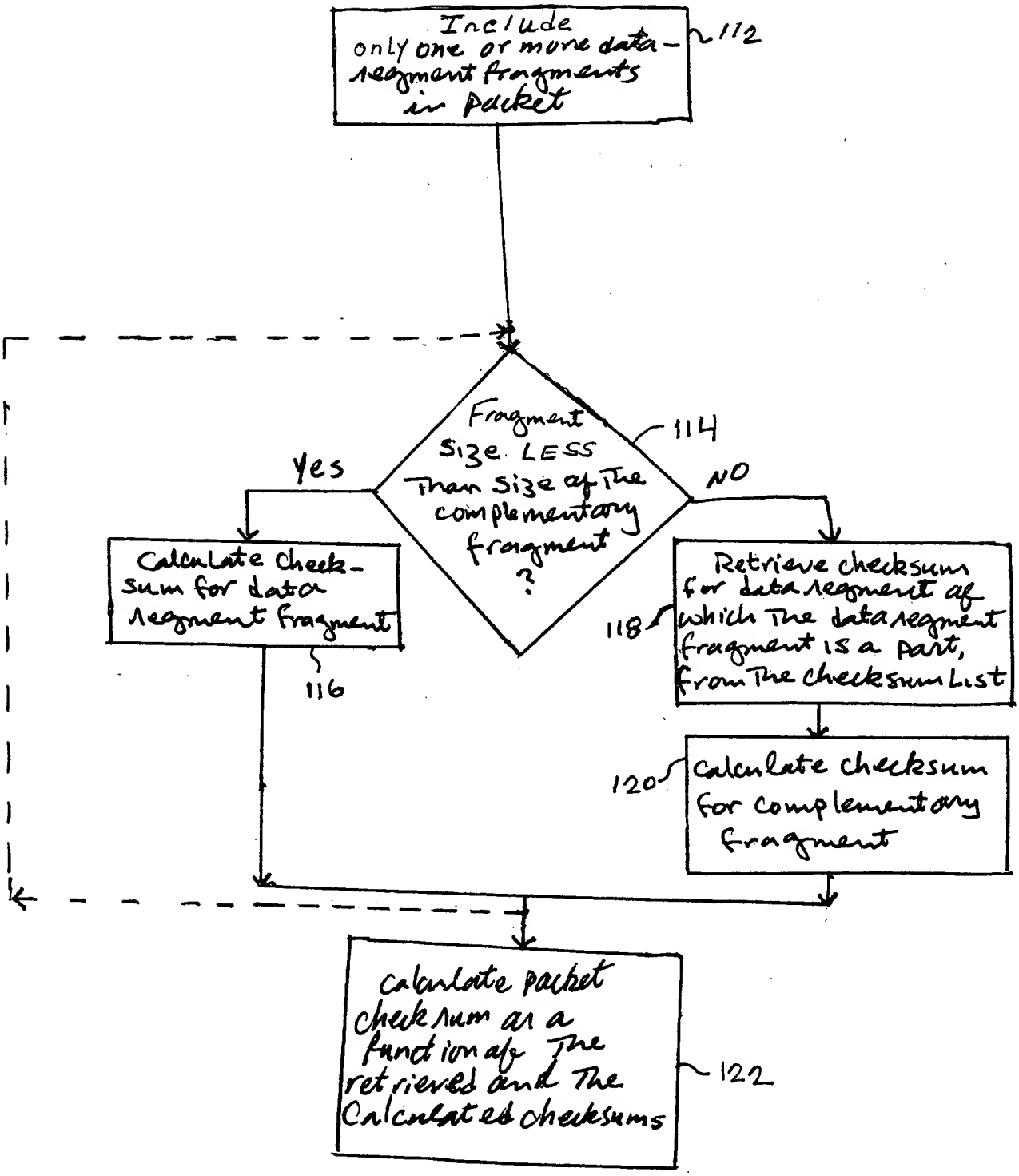

Include only one or more data-segment fragments in packet
112
Fragment Size LESS Than Size of The complementary fragment ?
114
Yes
NO
Calculate Checksum for data segment fragment
116
Retrieve checksum for data segment of which The data segment fragment is a part, from The checksum List
118
Calculate checksum for complementary fragment
120
Calculate packet checksum as a function of The retrieved and The Calculated checksums
122

FIG. 8

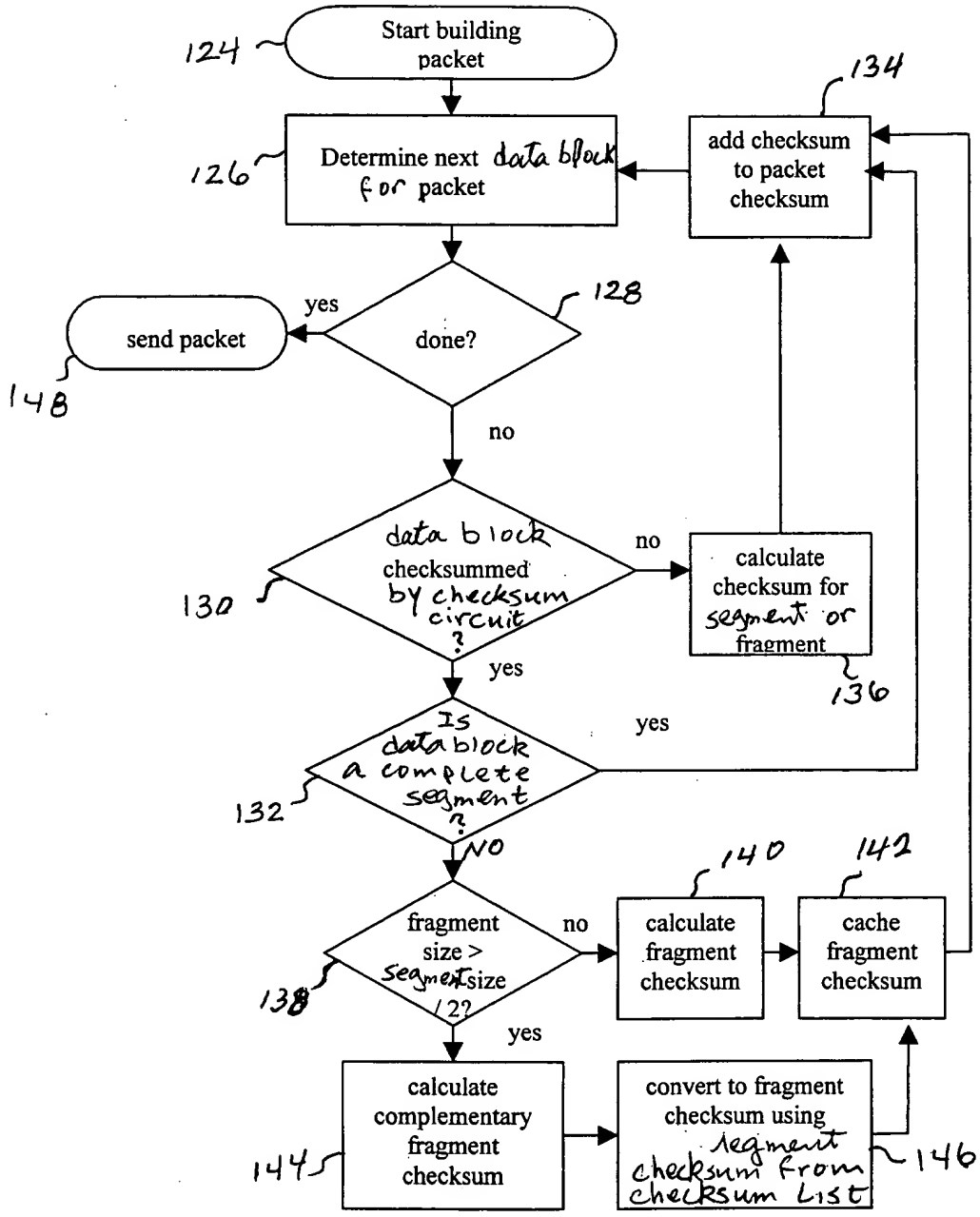

124
Start building packet
126
Determine next data block for packet
134
add checksum to packet checksum
128
done?
yes
send packet
148
no
130
data block checksummed by checksum circuit ?
no
calculate checksum for segment or fragment
136
yes
132
Is data block a complete segment ?
yes
NO
140
142
138
fragment size > segment size /2?
no
calculate fragment checksum
cache fragment checksum
yes
144
calculate complementary fragment checksum
convert to fragment checksum using segment checksum from checksum List
146

FIG. 9

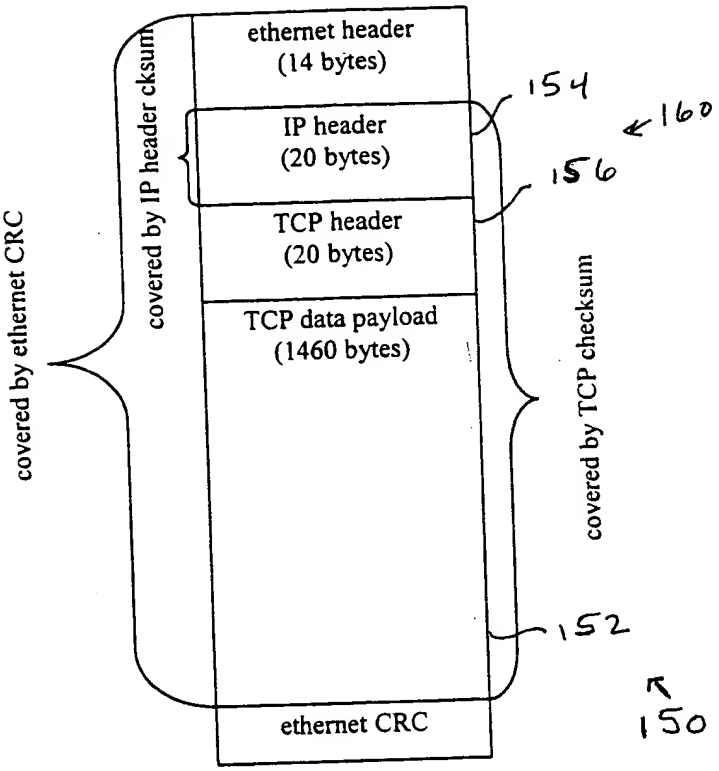


FIG. 10A

154

0	3	7	15	18	23	31
Version Number	Length	Service Type	Packet Length			
Identification				D F	M F	Offset
Time to Live		Transport	Header Checksum			
Source Address						
Destination Address						
Options (optional)						Padding

FIG. 10B

0	3	7	15	18	23	31
Source Address						
Destination Address						
Zero		Transport Protocol	Packet Length			

158

FIG. 10C

packet number	relative segment numbers	cumulative bytes	modulo 512	fragment software checksummed	software checksum size
0	0-2	1460	436	outer	76
1	2-5	2920	360	outer	152
2	5-8	4380	284	outer	228
3	8-11	5840	208	inner	208
4	11-14	7300	132	inner	132
5	14-17	8760	56	inner	56

FIG. 11

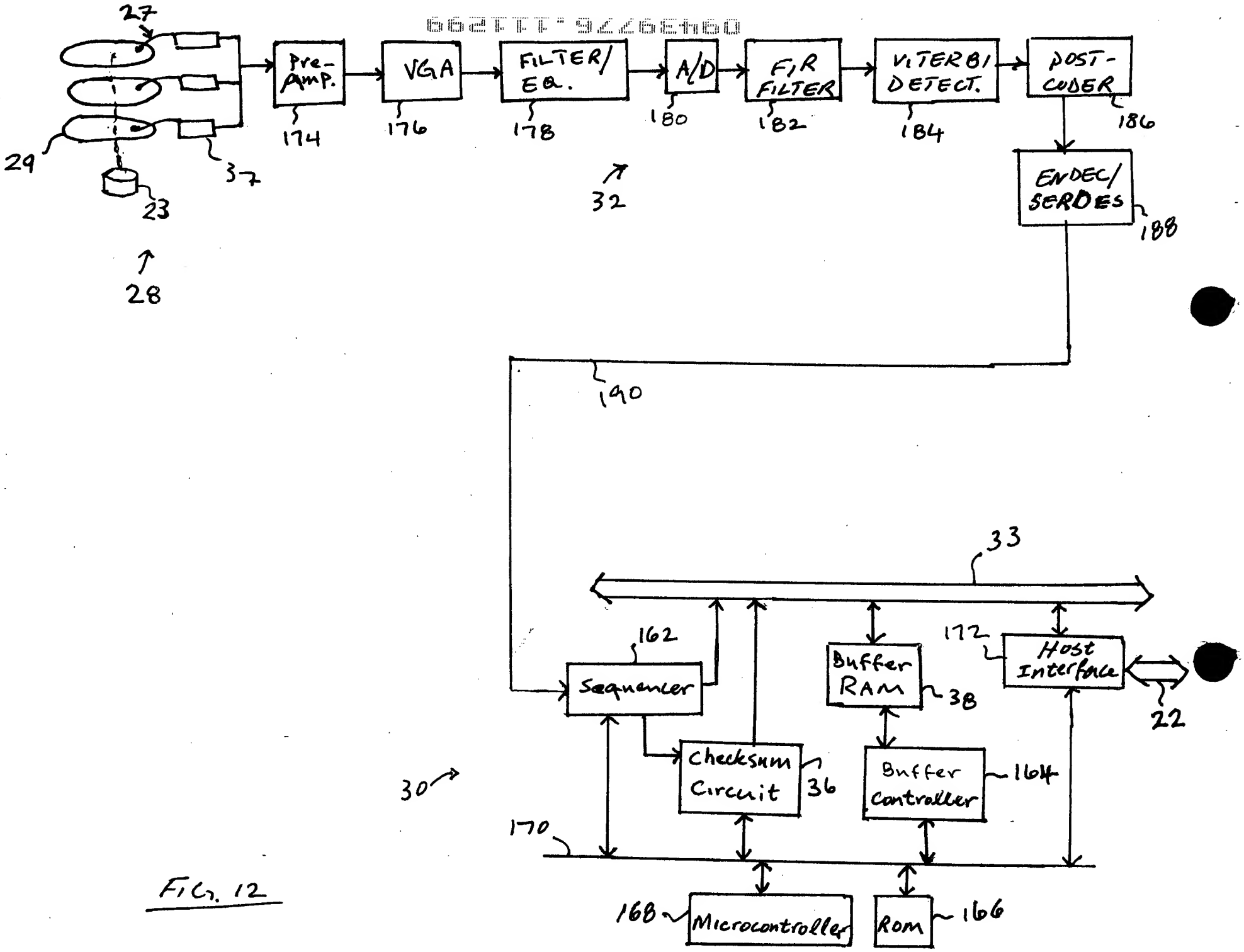

27
29
37
23
28
Pre-Amp.
174
VGA
176
FILTER/EQ.
178
A/D
180
FIR FILTER
182
VITERBI DETECT.
184
POST-CODER
186
ENDEC/SERDES
188
32
190
33
162
Sequencer
Buffer RAM
38
172
Host Interface
22
Checksum Circuit
36
Buffer Controller
164
30
170
168
Microcontroller
ROM
166

FIG. 12

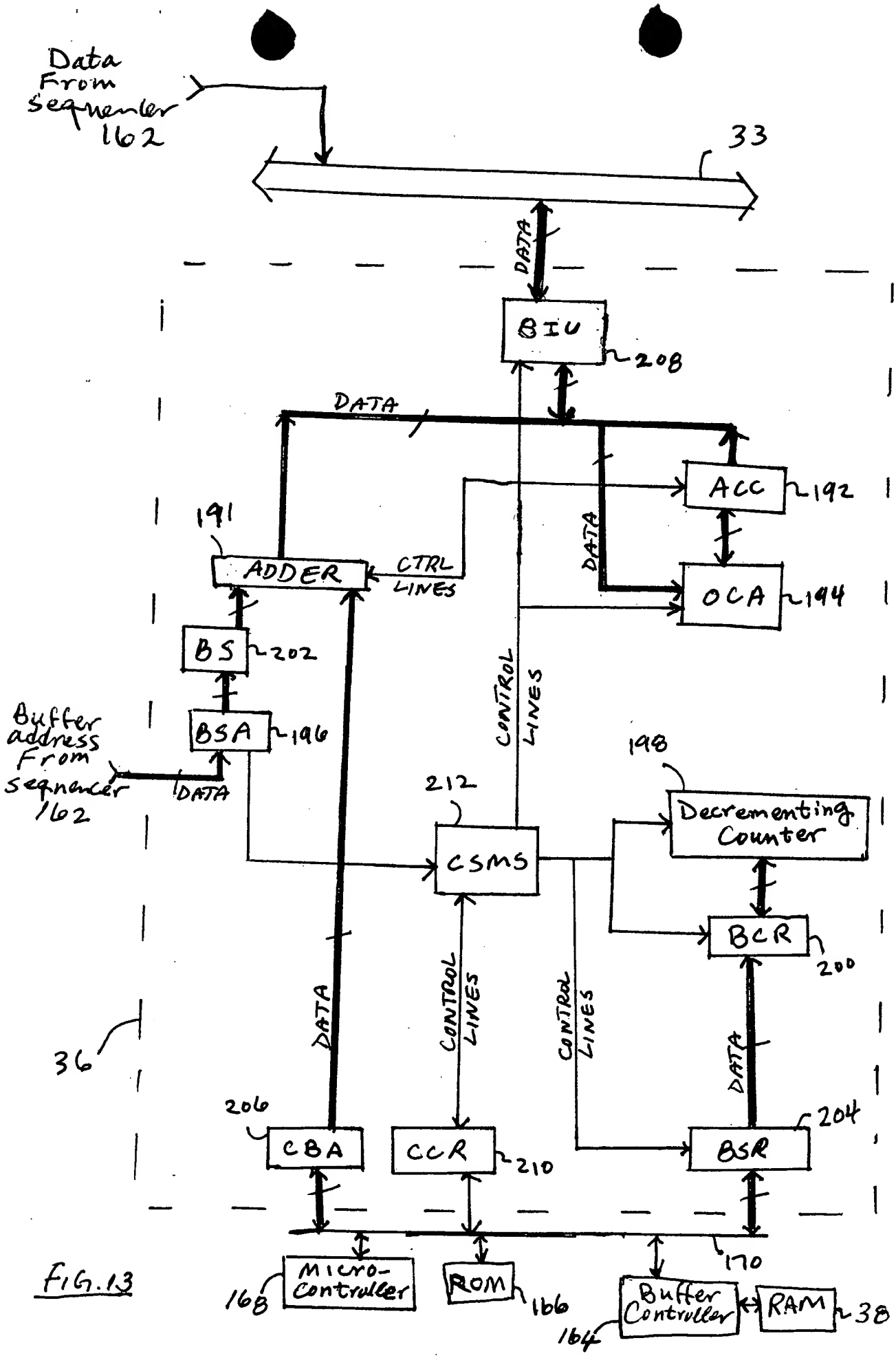

Data From Sequencer 162
33
DATA
BIU
208
DATA
ACC
192
191
ADDER
CTRL LINES
DATA
OCA
194
BS
202
BSA
196
Buffer address From sequencer 162
DATA
CONTROL LINES
198
212
Decrementing Counter
CSMS
BCR
200
36
DATA
CONTROL LINES
CONTROL LINES
DATA
206
204
CBA
CCR
210
BSR
170
168
Micro-controller
ROM
166
Buffer Controller
164
RAM
38

FIG. 13

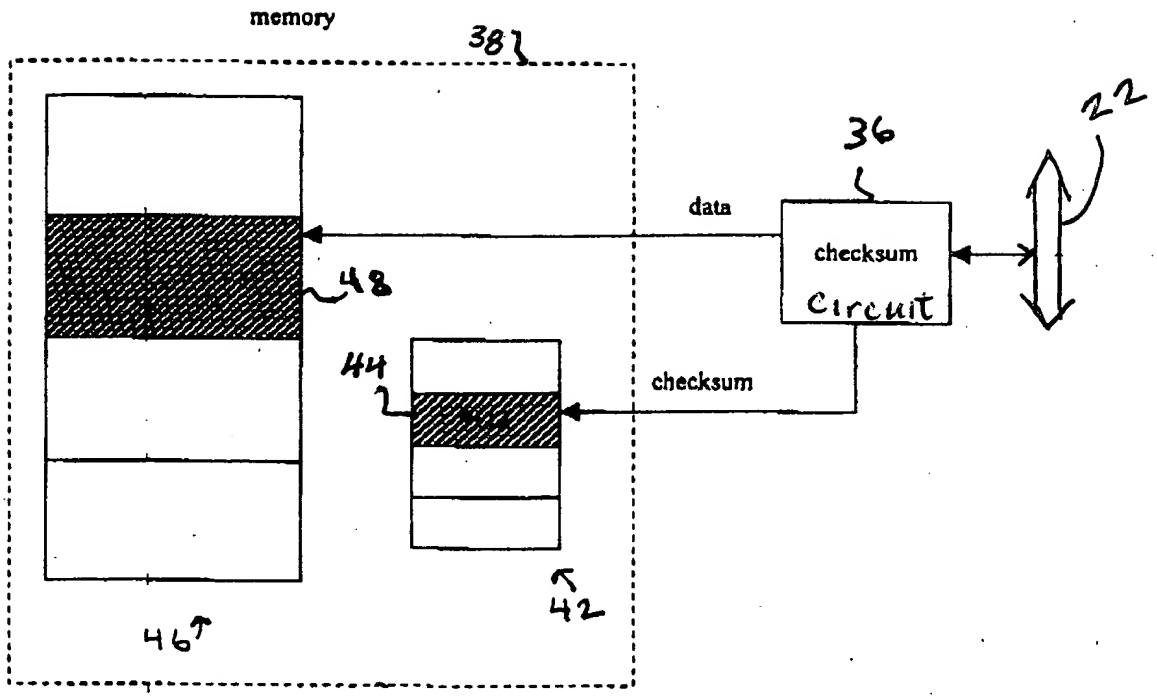
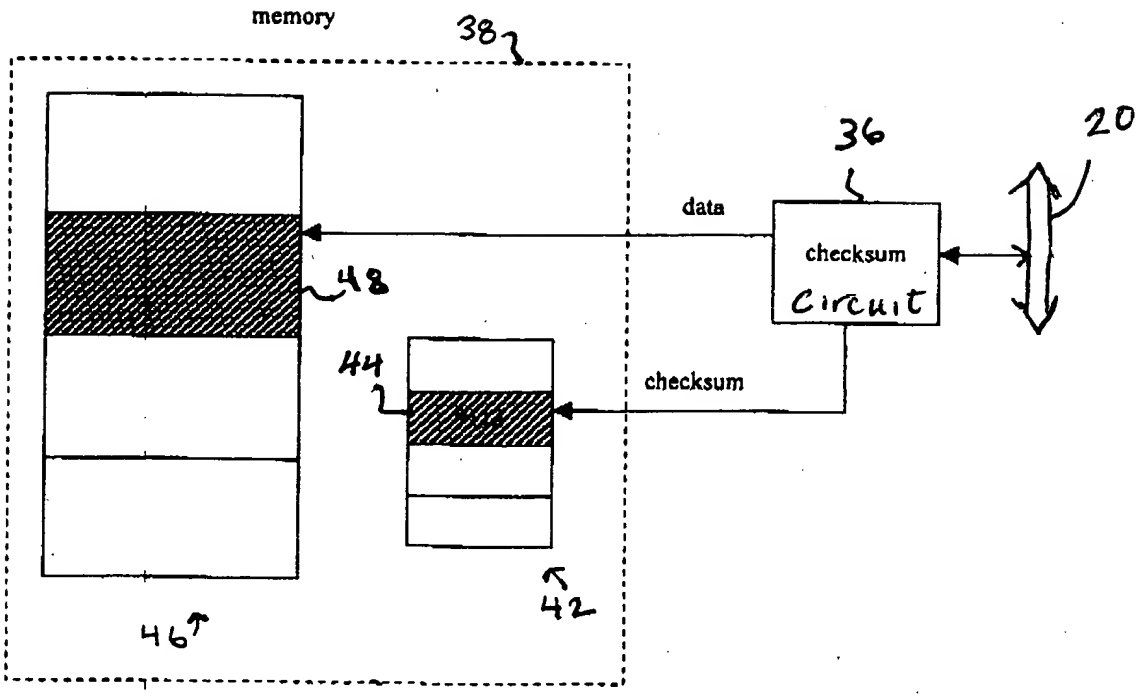


FIG. 14



15

FIG. 15